claims 1-20, being all the pending claims, are now deemed in condition for allowance. Reconsideration to that end is respectfully requested.

The Examiner has rejected claims 1, 5, 6, and 11 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,353,877, issued to Duncan et al (hereinafter referred to as "Duncan"). This ground of rejection is respectfully traversed for the reasons provided below.

"It is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention, and that such a determination is one of fact". *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81, 90 (Fed. Cir. 1986). The rejection of claims 1, 5, 6, and 11 are respectfully traversed, because the cited prior art does not "meet every element of the claimed invention".

In making his rejection of claims 1 and 6, the Examiner finds:

> ....said level two cache memory having cache storage (Fig. 2, data store 46)

This finding is clearly erroneous. Duncan states at column 6, lines 22-23:

> ....a primary cache that includes instructions store 44 and data store 46.

Clearly, data store 46 is a portion of the primary (i.e., level one) cache memory and not the secondary (i.e., level two) cache memory. The rejection is respectfully traversed as based upon this clearly erroneous finding of fact.

The Examiner further finds:

"and tag storage (Fig. 2, duplicate tag store 54), ..."

This finding is also clearly erroneous. Duncan states at column 7, lines 30-32:

> The use of a duplicate tag store 54 facilitates a determination as to the contents of the B-cache of the processor.

Thus, it is apparent that duplicate tag store 54 is associated with B-cache 52 (which the Examiner has called the "level three memory"). The Examiner has made another clearly erroneous finding of fact.

The invention is further limited by separate and dedicated paths between the system bus and each of the memory tag store and the data store of the level two cache. This can be readily seen in Applicants' Fig. 4. The advantages of this approach are discussed at page 14, lines 8-12, of the specification. This feature is not found in Duncan. The Examiner states:

> ....the improvement comprising a first dedicated path between said system bus and said cache storage (Fig. 2, processor chip 40 has direct path to bus 20) and a second dedicated path between said system bus and said tag storage (Fig. 2, duplicate tag store 54 has direct path to bus 20).

Neither "processor chip 40" nor "duplicate tag store 54" is coupled to "system bus 20". Both are coupled to "Bus Control Logic 58". Therefore, the assertion that Duncan somehow meets the claim is clearly erroneous on its face from the statement of the Examiner.

The rejection of claims 1 and 6 is respectfully traversed as based upon a plurality of clearly erroneous findings of fact.

The Examiner has further rejected claim 5 as being anticipated by Duncan. This rejection is respectfully traversed because it is incorrect as a matter of law. Claim 5 depends from claim 4, which depends from claim 3, which depends from claim 2, which depends from claim 1. Therefore, claim 5 contains all of the limitations of claims 1, 2, 3, and 4, in addition to the unique limitations of claim 5. Claim 2 is limited by "control logic responsively coupled to said cache storage and said tag storage which provides the highest priority for said SNOOPing". The Examiner admits that Duncan does not meet this limitation, stating:

> However, Duncan does not specifically teach a control logic which provides the highest priority for a SNOOPing as recited in the claims.

As a result, claim 5 admittedly contains at least one limitation not found in Duncan. The rejection of claim 5 is respectfully traversed because it is incorrect as a matter of law.

In rejecting claim 11, the Examiner states:

> As per claim 11, Duncan discloses the claimed invention as detailed per claim 1 above.

As established above, the rejection of claim 1 is based upon a plurality of clearly erroneous findings of fact. On that basis alone, the rejection of claim 11 may be respectfully traversed.

Claim 11 is a method claim further limited by the "presenting" and "routing" steps. Duncan does not meet these limitations. In making his rejection, the Examiner states:

> ....(i.e., all devices coupled to system bus snoops the bus, including secondary cache)(col. 8, lines 10-12).....

This finding is clearly erroneous because the citation does not support the Examiner's finding of "including secondary cache". Furthermore, Fig. 2 specifically shows that "secondary cache 48" is not coupled to "system bus 20". In fact, Fig. 2 shows "secondary cache 48" only coupled to "Instruction Store 44" and "Data Store 46". Therefore, the Examiner's assertion is not supported by the reference and his statement is clearly erroneous to the extent that he says that it does.

Similarly, the claimed "routing" step of claim 11 requires routing to the "tag memory" of the "level two cache". Instead of addressing this limitation, the Examiner states that Duncan routes the SNOOP request to the "B-cache" (i.e., level three) duplicate tag storage 46. Again, the rejection of claim 11 is

respectfully traversed as based upon a plurality of clearly erroneous findings of fact.

Claims 2-4, 8, 10, 12, and 14-15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan in view of U.S. Patent No. 5,426,765, issued to Stevens et al. (hereinafter referred to as "Stevens"). This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as specified by MPEP 2143.

Specifically, the Examiner states:

> As per claims 2 and 12, Duncan discloses the claimed invention as detailed above in the previous paragraphs.

Having previously established the plurality of clearly erroneous findings of fact, the rejection of claims 2 and 12 is respectfully traversed.

Furthermore, the Examiner clearly erroneously states:

> Stevens et al. disclose a control logic which provides the highest priority for a SNOOPing (col. 4, lines 23-32).

This is not the general case for Stevens which states at column 4, lines 46-48:

> After an initial arbitration, if any, the processor and snoop access alternate tag access if both processor and snoop accesses are active.

Thus, the general case is that Stevens alternates processor and snoop requests, rather than granting snoop requests higher priority as is limiting of the claims.

Furthermore, utilization of the system bus 20 of Duncan is controlled by Arbiter 35 (see Fig. 1). There is no showing that Duncan transfers any snoop request via system bus 20. In addition, there is no showing that Arbiter 35 has or could have any provision for controlling snoop requests transferred over system bus 20, if it did. The rejection of claims 2 and 12 is respectfully traversed.

In rejecting claim 3, the Examiner states:

> As per claim 3, Duncan discloses a level two cache memory further comprising a duplicate tag memory (Fig. 2, duplicate tag store 54).

This finding is clearly erroneous factually as explained above. Duplicate tag store 54 is associated with the B-cache 52, which the Examiner considers the level three memory. Duncan supports this at column 7, lines 30-32.

His finding is also objectionable as a matter of law. The Examiner has read "duplicate tag store 54" as the level two tag store in his rejection of claim 1. Now he impermissibly redefines the "duplicate tag store 54" in rejecting claim 3 which depends from claim 1 as a different claim element. The rejection of claim 3 is respectfully traversed as based upon clearly erroneous findings of fact and incorrect application of controlling law.

In rejecting claims 10, 14, and 15, the Examiner clearly erroneously finds that Duncan has a "SNOOP request". He continuously cites column 8, lines 11-20, which says nothing of a "SNOOP request". Duncan does not provide for a "SNOOP request" but seems to imply that various devices constantly SNOOP for cache consistency problems. These rejections are respectfully traversed as based upon clearly erroneous findings of fact.

The Examiner has rejected claims 7, 9, 13, and 16-20 under 35 U.S.C. 103(a) as being unpatentable over Duncan in view of Stevens and further in view of U.S. Patent No. 6,457,087, issued to Fu (hereinafter referred to as "Fu"). This rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as required by MPEP 2143. In addition to the numerous clearly erroneous findings of fact and errors or law explained above, the Examiner has not provided motivation to make the alleged combination. Specifically, he states:

> ....because it would have <u>provided flow control</u> of read and write transaction (sic) in the system by searching the caches for the intended data (col. 6, lines 38-48) and improved <u>cache coherency</u> in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system (col. 31, lines 11-16) as taught by Fu. (Emphasis added)

These allegations appear to be inconsistent with the Examiner's rejections. If Duncan and/or Stevens do not have "flow control"

and "cache coherency" without Fu, they are themselves inoperative, and thus not appropriate as prior art. If Duncan and/or Stevens do have "flow control" and "cache coherency" without Fu, then the alleged combination is not needed and therefore not motivated. In either case, the Examiner has not met his burden of showing motivation as required by MPEP 2143. Thus, this rejection is respectfully traversed.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-20, being the only pending claims.

Please charge any deficiencies or credit any over payment to Deposit Account 14-0620.

Respectfully submitted,

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By their attorney,

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